

CDCL3000C0-0002R7STZ

ULTRACAPACITOR CELL



SERIES

CDCL ULTRACAPACITOR CELL

| Rev | Date Revision of historical records | | |
|---------|-------------------------------------|-------------------|--|
| V2020-1 | 24-02-20 | The First Release | |
| V2020-2 | 12-05-20 | Version Update | |

SCOPE

These are the specifications of SPSCAP (Electric Double Layer Capacitor) which you are using, please review this document and approve it.

FEATURES

Low ESR & High Power Density

Over 1,000,000 duty cycles

Threaded connection

APPLICATIONS

EV/HEV

Hybrid driven trains

Mass transportation braking energy recovery system

Heavy duty machinery

Locomotive engine start system

Document number: DT14-08-201912 Rev. & Date: V2020-2 2020.05.12 2.7V 3000F CDCL-STZ



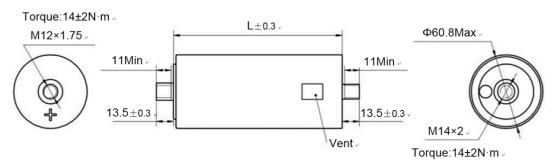
CONSTRUCTION AND DIMENSIONS

1) Construction

Inside structure: fold anode and cathode electrode with separator

Outer structure: aluminum case, insulating sleeve

2) Dimensions



| PART NUMBER | DIMENSION(mm) | | |
|----------------------|---------------|--|--|
| PART NOWIDER | L±0.3 | | |
| CDCL3000C0-0002R7STZ | 138.0 | | |

| PART NUMBER NAMING SYSTEM | | | | | | | | | | |
|---------------------------|--------------------------|-------------------------|---------|--|-------------------|------|-----------------|---|------------|------------|
| | CDCL | 3000 | 0 C 0 | | - | 0002 | R | 7 | STZ | |
| Pro | oduct Series | Nominal Capacitance (F) | | | Rated Voltage (V) | | Terminal Design | | | |
| С | Cell | 3000 | 3000 | | | 0002 | 2 | | ST | Threaded |
| D | Electric double layer | С | Decimal | | Dash | R | Decimal | | connection | connection |
| С | Cylindrical | 0 | 0.0 | | | 7 | 0. | 7 | Z | Standard |
| L | Large | U | | | | | 0.7 | L | Design | |

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| GENERAL CHARACTERISTICS | |
|--|------------------|
| Items | Specification |
| Rated Voltage (V DC) | 2.7 |
| Surge Voltage (V DC) | 2.85 |
| Operating Temp. (°C) | -40 ∼ +65 |
| Rated Capacitance (F) | 3000 |
| Capacitance Tolerance | 0% ~ 20% |
| ESR Max. (AC@1KHz, mΩ) | 0.22 |
| ESR Max. (DC, $m\Omega$) | 0.29 |
| Maximum Continuous Current (ΔT=15°C, A) | 129 |
| Maximum Continuous Current (ΔT=40°C, A) | 211 |
| Maximum Peak Current (A) (1s) | 2166 |
| Max.LC (Room Temp. after 72hrs, mA) | 5.2 |
| Typical Thermal Resistance (R _{th} , Housing, °C/W) | 3.1 |
| Typical Thermal Capacitance (C _{th} , J/°C) | 645 |
| Weight (g) | 548 |
| Energy Stored (Wh) | 3.04 |



RELIABILITY SPECIFICATIONS

| ITEM | | SPECIFICATION | | CONDITION | |
|--------------------------|-------------|---------------|-----------------------------------|--|--|
| Temp. Characteristics | Capacitance | Chara 1 | Change within 5% of Initial Value | Step 1:+25±2°C, 1h Step 2:+65±2°C, 1h | |
| | ESR | Step. 1 | Change within 50% of rated value | | |
| | Capacitance | C 1 0 | Change within 5% of Initial Value | | |
| | ESR | Step. 2 | Change within 50% of rated value | | |
| | Capacitance | C 1 0 | Change within 5% of Initial Value | Step 3: -25±2°C, 1h | |
| | ESR | Step. 3 | Change within 50% of rated value | Step 4: -40±2°C, 1h | |
| | Capacitance | | Change within 5% of Initial Value | | |
| | ESR | Step. 4 | Change within 50% of rated value | | |
| | Capacitance | Initial Va | lue | | |
| Vibration Test | ESR | Initial Va | lue | ISO16750-3 Table 14 | |
| | Appearance | Not Mark | ked Defect | | |
| Thermal Cycle | Capacitance | Initial Va | lue | Temp.: -40°C ~ 65°C Cycle times: 6 Test Time(One Cycle): -40°C 2hrs, +65°C 2hrs, Temp change 2hrs | |
| | ESR | Initial Va | lue | | |
| | Appearance | Not Mark | ked Defect | | |
| | Capacitance | Change w | rithin 20% of Initial Value | Temp.: +40±2°C | |
| Humidity Test | ESR | Change w | vithin 100% of Initial Value | Humidity: 90-95%RH | |
| | Appearance | Not Mark | ked Defect | Test Time: 240±8hrs | |
| | Capacitance | Change w | vithin 20% of Initial Value | Temp.: +65±2℃ | |
| DC Life | ESR | Change w | vithin 100% of Initial Value | Voltage: 2.7V | |
| | Appearance | Not Mark | ked Defect | Time: 1,500hrs | |
| Shelf Life | Capacitance | Change w | rithin 20% of Initial Value | | |
| | ESR | Change w | vithin 100% of Initial Value | Temp.: +70±2°C Time: 1,000hrs | |
| | Appearance | Not Mark | ked Defect | ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,, | |
| Cycle Life | Capacitance | Change w | vithin 20% of Initial Value | Tomp 25 2°C | |
| | ESR | Change w | vithin 100% of Initial Value | Temp.: +25±2°C Cycles times: | |
| | Appearance | Not Mark | ced Defect | 1,000,000 | |



MEASURING METHOD

- 1) Charge and Discharge procedure (Figure 1)
 - A) Charge the capacitor using constant current I to rated voltage V₀
 - B) Keep rated voltage 5 mins
 - C) Discharge the capacitor using constant current I to half rated voltage, record discharge time T₁ during voltage change from V₁to V₂
 - D) Rest 2-5s, record voltage change ΔV
 - E) Discharge it to a very low voltage around 0.01V
 - F) $V_1 = 85\% V_0 V_2 = 50\% V_0$



 $C = I \cdot T_1 / (V_1 - V_2)$

C: Capacitance (F)

I: Constant Discharge Current (A)

T₁: Discharge Time (S)

 V_1 - V_2 : Voltage Change (V)



DC ESR= $\Delta V/I$

DC ESR: DC Equivalent Series Resistance (Ω)

ΔV: Voltage Change (V)

I: Constant Discharge Current (A)

4) AC ESR

Measure AC ESR using LCR meter

Frequency: 1KHz

Voltage: fully discharge

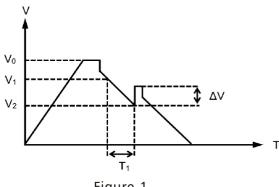


Figure 1

REMARK: SPSCAP EDLC SHOULD BE DISCHARGED WITH RESISTOR FOR AT LEAST 12 HOURS BEFORE MEASUREMENT OF CAPACITANCE OR ESR.

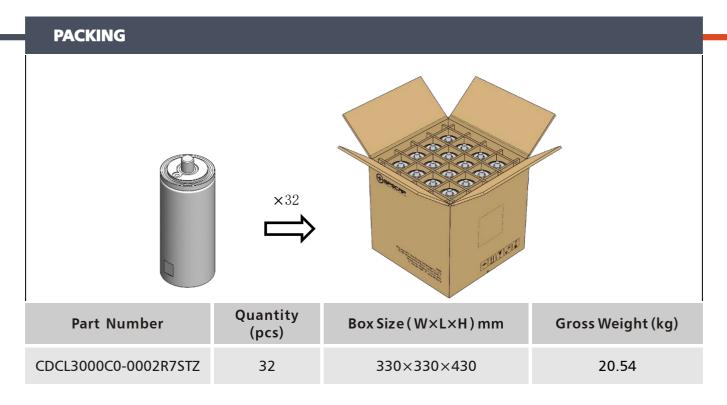


NOTES AND CAUTION

Please notice below points when you start use SPSCAP.

- 1) The SPSCAP gets polarity through aging/testing process before it is packed, so please mount it in accordance with its polarity to maintain the best condition;
- 2) Please only apply SPSCAP at rated voltage. If you apply more than rated voltage, capacitor will be damaged or broken due to electrolyte inside will be electrolyzed;
- 3) Ambient temperature greatly affects the lifetime of the capacitor, by reducing the temperature by 10°C, lifetime can be approximately doubled;
- 4) Storage: In long term storage, please store SPSCAP in following condition:
 - Temp.: 15 ~ 35°C
 - Humidity: 40 ~ 75 %RH
 - No-dust, non-acidic and/or non-alkaline atmosphere
 - Avoid direct sun light
- 5) Do not disassemble SPSCAP. It contains electrolyte;
- 6) Avoid serious mechanical impacts onto capacitor, such as force or twist capacitor;
- 7) Please contact us if you want to subject SPSCAP to severe vibrating conditions exceeding rated specification;
- 8) Please contact us if you want to connect a certain number of single capacitor to make a module;
- 9) Over-rated voltage may be applied to a single SPSCAP in series connection due to the deviation of capacitance and ESR of each SPSCAP. Please inform us if you are using SPSCAP in series connection and please design so as not to apply over-rated voltage to each capacitor, and use SPSCAP from same date code/lot.





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