

CDCL1200C0-0002R7STZ

ULTRACAPACITOR CELL



SERIES	CDCL ULTRACAPACITOR CELL
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Rev	Date	Revision of historical records
V2020-1	24-02-20	The First Release
V2020-2	12-05-20	Version Update

SCOPE

These are the specifications of SPSCAP (Electric Double Layer Capacitor) which you are using, please review this document and approve it.

- FEATURES**
- Low ESR & High Power Density
 - Over 1,000,000 duty cycles
 - Threaded connection

- APPLICATIONS**
- EV/HEV
 - Hybrid driven trains
 - Mass transportation braking energy recovery system
 - Heavy duty machinery
 - Locomotive engine start system

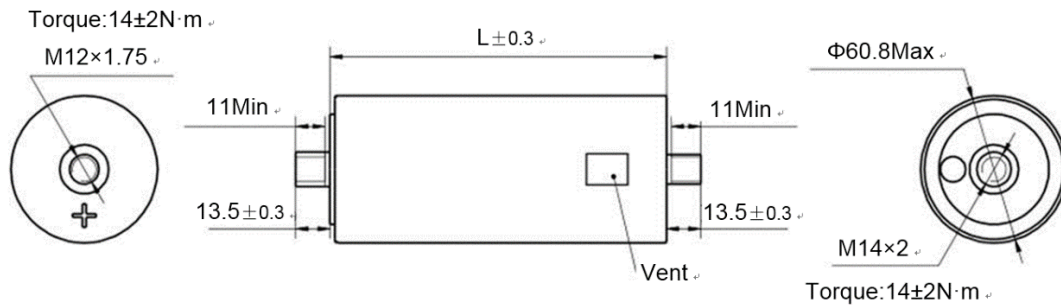
CONSTRUCTION AND DIMENSIONS

1) Construction

Inside structure: fold anode and cathode electrode with separator

Outer structure: aluminum case, insulating sleeve

2) Dimensions



PART NUMBER	DIMENSION(mm)
	$L \pm 0.3$
CDCL1200C0-0002R7STZ	74.0

PART NUMBER NAMING SYSTEM

CDCL	1200	C	0	-	0002	R	7	STZ
Product Series		Nominal Capacitance (F)		Dash	Rated Voltage (V)		Terminal Design	
C	Cell	1200	1200		0002	2	ST	Threaded connection
D	Electric double layer	C	Decimal		R	Decimal		
C	Cylindrical	0	0.0		7	0.7	Z	Standard Design
L	Large							

GENERAL CHARACTERISTICS

Items	Specification
Rated Voltage (V DC)	2.7
Surge Voltage (V DC)	2.85
Operating Temp. (°C)	-40 ~ +65
Rated Capacitance (F)	1200
Capacitance Tolerance	0% ~ 20%
ESR Max. (AC@1KHz, mΩ)	0.40
ESR Max. (DC, mΩ)	0.58
Maximum Continuous Current ($\Delta T=15^{\circ}\text{C}$, A)	72
Maximum Continuous Current ($\Delta T=40^{\circ}\text{C}$, A)	117
Maximum Peak Current (A) (1s)	955
Max.LC (Room Temp. after 72hrs, mA)	2.5
Typical Thermal Resistance (R_{th} , Housing, °C/W)	5.0
Typical Thermal Capacitance (C_{th} , J/°C)	338
Weight (g)	293
Energy Stored (Wh)	1.22

RELIABILITY SPECIFICATIONS

ITEM		SPECIFICATION		CONDITION
Temp. Characteristics	Capacitance	Step. 1	Change within 5% of Initial Value	Step 1: +25±2°C, 1h Step 2: +65±2°C, 1h Step 3: -25±2°C, 1h Step 4: -40±2°C, 1h
	ESR		Change within 50% of rated value	
	Capacitance	Step. 2	Change within 5% of Initial Value	
	ESR		Change within 50% of rated value	
	Capacitance	Step. 3	Change within 5% of Initial Value	
	ESR		Change within 50% of rated value	
	Capacitance	Step. 4	Change within 5% of Initial Value	
	ESR		Change within 50% of rated value	
Vibration Test	Capacitance	Initial Value		ISO16750-3 Table 14
	ESR	Initial Value		
	Appearance	Not Marked Defect		
Thermal Cycle	Capacitance	Initial Value		Temp.: -40°C ~ 65°C Cycle times: 6 Test Time(One Cycle): -40°C 2hrs, +65°C 2hrs, Temp change 2hrs
	ESR	Initial Value		
	Appearance	Not Marked Defect		
Humidity Test	Capacitance	Change within 20% of Initial Value		Temp.: +40±2°C Humidity: 90-95%RH Test Time: 240±8hrs
	ESR	Change within 100% of Initial Value		
	Appearance	Not Marked Defect		
DC Life	Capacitance	Change within 20% of Initial Value		Temp.: +65±2°C Voltage: 2.7V Time: 1,500hrs
	ESR	Change within 100% of Initial Value		
	Appearance	Not Marked Defect		
Shelf Life	Capacitance	Change within 20% of Initial Value		Temp.: +70±2°C Time: 1,000hrs
	ESR	Change within 100% of Initial Value		
	Appearance	Not Marked Defect		
Cycle Life	Capacitance	Change within 20% of Initial Value		Temp.: +25±2°C Cycles times: 1,000,000
	ESR	Change within 100% of Initial Value		
	Appearance	Not Marked Defect		

MEASURING METHOD

1) Charge and Discharge procedure (Figure 1)

- A) Charge the capacitor using constant current I to rated voltage V_0
- B) Keep rated voltage 5 mins
- C) Discharge the capacitor using constant current I to half rated voltage, record discharge time T_1 during voltage change from V_1 to V_2
- D) Rest 2-5s, record voltage change ΔV
- E) Discharge it to a very low voltage around 0.01V
- F) $V_1 = 85\% V_0$ $V_2 = 50\% V_0$

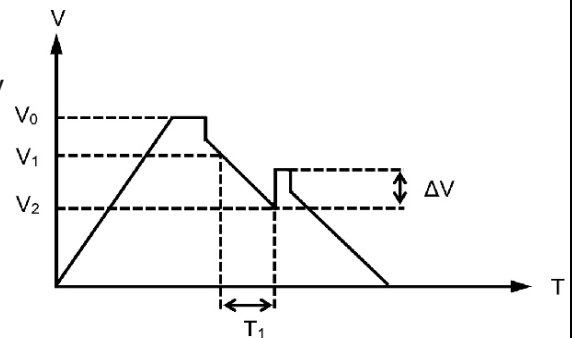


Figure 1

2) Capacitance

$$C = I \cdot T_1 / (V_1 - V_2)$$

C: Capacitance (F)

I: Constant Discharge Current (A)

T_1 : Discharge Time (S)

$V_1 - V_2$: Voltage Change (V)

3) DC ESR

$$\text{DC ESR} = \Delta V / I$$

DC ESR: DC Equivalent Series Resistance (Ω)

ΔV : Voltage Change (V)

I: Constant Discharge Current (A)

4) AC ESR

Measure AC ESR using LCR meter

Frequency: 1KHz

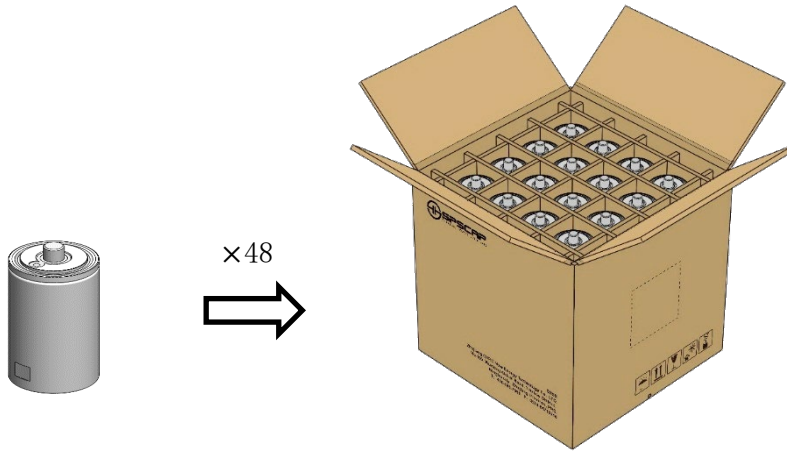
Voltage: fully discharge

REMARK: SPSCAP EDLC SHOULD BE DISCHARGED WITH RESISTOR FOR AT LEAST 12 HOURS BEFORE MEASUREMENT OF CAPACITANCE OR ESR.

NOTES AND CAUTION

Please notice below points when you start use SPSCAP.

- 1) The SPSCAP gets polarity through aging/testing process before it is packed, so please mount it in accordance with its polarity to maintain the best condition;
- 2) Please only apply SPSCAP at rated voltage. If you apply more than rated voltage, capacitor will be damaged or broken due to electrolyte inside will be electrolyzed;
- 3) Ambient temperature greatly affects the lifetime of the capacitor, by reducing the temperature by 10°C, lifetime can be approximately doubled;
- 4) Storage: In long term storage, please store SPSCAP in following condition:
 - Temp.: 15 ~ 35°C
 - Humidity: 40 ~ 75 %RH
 - No-dust, non-acidic and/or non-alkaline atmosphere
 - Avoid direct sun light
- 5) Do not disassemble SPSCAP. It contains electrolyte;
- 6) Avoid serious mechanical impacts onto capacitor, such as force or twist capacitor;
- 7) Please contact us if you want to subject SPSCAP to severe vibrating conditions exceeding rated specification;
- 8) Please contact us if you want to connect a certain number of single capacitor to make a module;
- 9) Over-rated voltage may be applied to a single SPSCAP in series connection due to the deviation of capacitance and ESR of each SPSCAP. Please inform us if you are using SPSCAP in series connection and please design so as not to apply over-rated voltage to each capacitor, and use SPSCAP from same date code/lot.

PACKING


Part Number	Quantity (pcs)	Box Size (W×L×H) mm	Gross Weight (kg)
CDCL1200C0-0002R7STZ	48	330×330×430	17.06

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NINGBO CRRC NEW ENERGY TECHNOLOGY CO.,LTD.

Add: No.199 Shidai Road,Wuxiang Town,Yinzhou District,
Ningbo,Zhejiang,China

Email: info@spscap.com

Website: www.spscap.com